REMARKS

Claims 34-37, 46 and 53-58 are pending in the present application.

Information Disclosure Statement

An Information Disclosure Statement has been filed on October 30, 2007, in connection with this application. The Information Disclosure Statement has been entered into the image file wrapper of this application on the U.S. Patent Office website. **The Examiner is respectfully requested to acknowledge receipt of the Information Disclosure Statement, and to confirm that the document listed thereon has been considered and will be cited of record in the present application.**

Claim Rejections-35 U.S.C. 103

Claims 34-37, 46, 53-56 and 58 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Lin et al. reference (U.S. Patent No. 5,239,198) in view of the Okuno et al. reference (U.S. Patent No. 6,063,646). This rejection is respectfully traversed for the following reasons.

The semiconductor device of claim 34 includes a CSP (chip size package) type semiconductor device mounted on the backside surface of a base plate of a BGA (ball grid array) type semiconductor device. The CSP type semiconductor device has a resin that covers the main surface of the semiconductor element. However, the resin does

not cover the side and back surfaces of the semiconductor element. That is, the side and back surfaces of the semiconductor element are exposed. The CSP type semiconductor device has a thickness less than a thickness of the corresponding plurality of bumps.

By employing of the semiconductor device as featured in claim 34, poor connections between the plurality of bumps and a printed circuit board on which the semiconductor device is mounted can be avoided or reduced. In addition, since side and back surfaces of the semiconductor element are not covered with resin, radiation of heat from the CSP type semiconductor device is not degraded, even in a case in which the CSP type semiconductor device is mounted in narrow space.

As emphasized previously, the Lin et al. reference does not disclose a CSP type semiconductor device having a semiconductor element. That is, passive electronic component 50 in Figs. 6 and 7 of the Lin et al. reference is merely a resistor, a diode, a decoupling capacitor, **or the like**. There is no description in the Lin et al. reference characterizing passive electronic component 50 as or including "a semiconductor chip".

In the Response to Arguments section bridging pages 7-8 of the Final Office Action dated August 21, 2007, the Examiner has merely asserted that: ***"The passive electronic component 50 as taught by Lin et al. is chip size package type semiconductor device. The chip type semiconductor device would be the passive component (a resistor, a capacitor, or a diode)".*** However, the Examiner has established no basis for characterizing a resistor, a capacitor or a diode as a CSP

(chip size package) type semiconductor device as would be understood by one of ordinary skill. Moreover, even assuming for the sake of argument that component 50 of the Lin et al. reference could be considered a CSP type semiconductor device (which Applicants do not concede), the Lin et al. reference does not teach, suggest, or address whether component 50 is covered with resin or not.

The Okuno et al. reference as secondarily relied upon merely discloses a CSP type semiconductor device. The Okuna et al. reference does not disclose or suggest the idea of mounting a CSP type semiconductor device on the backside of a base plate of a BGA type semiconductor device. One of ordinary skill thus would have no motivation to modify the structure in Fig. 6 of the Lin et al. reference to replace passive component 50 with a CSP type semiconductor device as shown in the Okuno et al. reference. For instance, heat radiation is not considered or addressed in either the Lin et al. or Okuno et al. references.

Accordingly, Applicants respectfully submit that the semiconductor device of claim 34 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 34-37, 46 and 58 is improper for at least these reasons. Applicant also respectfully submits that the semiconductor device of claim 53 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 53-56 is improper for at least somewhat similar reasons.

Claims 34, 37, 46, 53, 57 and 58 have been rejected under 35 U.S.C. 103(a) as

being unpatentable over the Inaba et al. reference (U.S. Patent No. 6,166,443) in view of the Okuno et al. reference. This rejection is respectfully traversed for the following reasons.

The structure in Fig. 9 of the primarily relied upon the Inaba et al. reference includes semiconductor element 24, the entirety of which is covered by resin 29. Element 24 is mounted on substrate 22. Moreover, the structure in Fig. 9 of the Inaba et al. reference is not specifically described as having element 24 mounted on a back surface of a base plate of a BGA type semiconductor device. Also, the manufacturing process as described with respect to the Fig. 9 embodiment of the Inaba et al. reference discloses that two chips are sealed by resin after mounting on substrate 22. The Inaba et al. reference does not disclose or suggest exposing back and side surfaces of a semiconductor element of a CSP type semiconductor device, in connection with the Fig. 9 embodiment as relied upon. One of ordinary skill thus would have no motivation to modify the Fig. 9 structure of the Inaba et al. reference in view of the secondarily relied upon Okuno et al. reference to meet the features of claim 34. Particularly, one of ordinary skill would have no motivation to omit resin 29 from an underside of substrate 22 in Fig. 9 of the Inaba et al. reference.

Accordingly, Applicants respectfully submit that the semiconductor device of claim 34 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 34, 37, 46, 57 and 58, is improper for at least these reasons. Applicants also respectfully submit that

the semiconductor device of claim 53 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 53 is improper for at least somewhat similar reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicants hereby petition for an extension of one (1) month to December 21, 2007, for the period in which to file a response to the outstanding Office Action. The required fee of $120.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE & WHITT, P.L.L.C.

Andrew J. Telesz, Jr.
Registration No. 33,581

11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283-0720
Facsimile No.: (571) 283-0740